

NBTI Degradation: A Problem or a Scare?

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Abstract

Negative Bias Temperature Instability (NBTI) has been identified as a major and critical reliability issue for PMOS devices in nano-scale designs. It manifests as a negative threshold voltage shift, thereby degrading the performance of the PMOS devices over the lifetime of a circuit. In order to determine the quantitative impact of this phenomenon an accurate and tractable model is needed. In this paper we explore a novel and practical methodology for modeling NBTI degradation at the logic level for digital circuits. Its major contributions include i) A SPICE level simulation to identify stress on PMOS devices under varying input conditions for various gate types and ii) a gate level simulation methodology that is scalable and accurate for determining stress on large circuits. We validate the proposed logic level simulation methodology by showing that it is accurate within 1% of the reference model. Contrary to many other papers in this area, our experimental results show that the overall delay degradation of large digital circuits due to NBTI is relatively small.

1. Introduction

Negative Bias Temperature Instability (NBTI) affects the p-MOSFET transistors. The degradation process caused by the generation of traps and partial recovery associated with reduction in traps is explained in [6], [8], [13]. NBTI degradation worsens at high temperatures, causing a larger shift in the threshold voltage. Further, over long period of time this threshold voltage shift can potentially cause a significant increase in delay of the p-MOSFET devices [4], [6].

NBTI degradation and its impact on circuit reliability and performance have become a key issue due to the continuous decrease of the transistor dimensions. A number of studies have been conducted to investigate the effect of NBTI on both digital and analog circuits [11], [2], [10], [7], [9]. Besides, many studies have also developed several design-time and run-time techniques to

cope with the NBTI degradation [3], [17], [7], [14]. These studies include the use of CAD tools for managing transistor degradation mechanism [3], the use of dynamic voltage scaling (DVS)[17], the use of data flipping to recover the static noise margin of the SRAM [7], and the use of device parameter tuning (V_{dd}, V_{th} and gate-size) in digital circuits [14].

Since, in the device community, NBTI is difficult to design around, an efficient and accurate model for predicting the performance degradation due to NBTI is urgently needed to design the circuits based on design-for-degradation techniques. Essentially, in digital circuits, which are more likely to suffer NBTI effects, several models of NBTI degradation in the literature have been used to capture the degradation behavior of all PMOS components as a function of their parameters and bias-voltages [11], [10], [14]. However, for large scale circuits, these device level NBTI stress models require extensive circuit simulation of every PMOS transistor in the circuit [17], [15], thus making them intractable and non-ideal. Design techniques that are meant to offset the effect of NBTI degradation using various methods, such as gate sizing [16], [5], require accurate prediction of degradation for gate or higher level designs of the logic circuits.

In this paper, a gate level simulation methodology which can model NBTI degradation of digital circuits accurately is developed. It employs a previously proposed device-level model [14] which has been experimentally verified to determine the degradation of p-MOSFET transistors in a gate over a period of given time. Our simulation technique can efficiently model V_{th} shift and delay of the devices for industrial scale benchmark circuits (ISCAS'85 and MCNC'91). More importantly, to identify the dynamic behavior of NBTI degradation due to the bias of a PMOS transistor which depends on the position of the PMOS transistor in the pull-up stack and also the logic input value, we use SPICE simulation to determine the input conditions and the extent of the stress for every PMOS transistor in the library of gates mapped onto the design. Our method can

also handle arbitrary stress pattern for any workload conditions. Hence it provides a better and more realistic prediction of the NBTI degradation in digital circuits. However, the model proposed in this paper is under the condition that all transistors in mapping gates have paths to ground so that we can construct the gate level model to predict the large scale degradation from practical SPICE simulation. In this phase, since we mainly focus on the effect of NBTI on circuit delay, other impacts such as voltage scaling, divergent paths, and power domain analysis are not considered.

The section 2 below provides an overview of the previously proposed NBTI modeling techniques and how they relate to our method. Section 3 gives the details of the proposed method and in Section 4 the experimental results are presented for numerous benchmark circuits. Finally, we conclude this research in Section 5.

2. Related Work

A comprehensive device-level predictive model covering both static and dynamic NBTI degradation is proposed by Vattikonda et. al. in [14]. This device level model is very accurate having been verified with the experimental data. The model calculates the amount of V_{th} shift due to NBTI degradation over time using the following equations:

Stress Phase:

$$\Delta V_{th} = \sqrt{K_v^2 (t - t_0)^{1/2} + \Delta V_{th0}^2} + \delta_v \quad (1)$$

Recovery Phase:

$$\Delta V_{th} = (\Delta V_{th} - \delta_v) \left(1 - \sqrt{\eta(t - t_0)/t} \right) \quad (2)$$

where,

$$K_v = A \cdot t_{ox} \cdot \sqrt{C_{ox} (V_{gs} - V_{th})} \cdot \left(1 - \frac{V_{gs}}{V_{gs} - V_{th}} \right) \cdot \exp\left(\frac{E_{ox}}{E_o}\right) \cdot \exp\left(\frac{E_a}{kT}\right) \quad (3)$$

A detailed explanation of this predictive model and the technology specifications are dealt within the original paper [14]. Using these equations, V_{th} shift of every PMOS transistor in the digital circuit can be determined on a cycle-by-cycle basis. After simulating the circuit operation for certain time period, such as the specified lifetime, the increase in delay of each transistor can be calculated from the obtained V_{th} shift using the alpha-power law [1] model, which expresses the delay dependence on the threshold voltage as:

$$Delay \propto \frac{V_{dd}}{(V_{dd} - V_{th})^\beta} \quad (4)$$

Finally, the overall circuit delay can be obtained by using any timing analysis scheme based on the increased delay of

each transistor. The drawback of the above methodology is that the modern digital circuits operate at hundreds or even thousands of MHz and NBTI is a long term degradation process occurring over the lifetime of the unit which could be several years. Hence, simulating the circuit in a cycle-by-cycle style, till the end of specified lifetime, is difficult, if not impossible, due to the tremendous computation need.

An architecture level model proposed in [12] is based on the circuit area and offers no insight into the logic level performance degradation. As a result this is of little value to the circuit designers who want to mitigate the effects of NBTI during the design phase. At the device and logical level, effects of NBTI degradation were studied by Reddy et al. [11] but the study was limited to SRAM cells. Paul et al. [10] provide a predictive model for circuit level degradation, but it only considers static NBTI effects. Authors in [14] also propose a model for predicting the long-term degradation but in this model the PMOS transistors are assumed to be stressed periodically. Whereas in reality, the input patterns to the circuit are not periodical. Thus the assumption is prone to producing erroneous results.

The simulation method proposed in this paper builds upon the device level model from [14] (Eq(1) and Eq(2)). It is capable of handling any specified or arbitrary workload efficiently. The fact that the original model of [14] has been verified with the experimental data, we argue that the proposed method is rather accurate. Indeed the method proposed by us simulates the NBTI degradation on a cycle-by-cycle basis and the assumption of periodic stress is relaxed. Finally, with a curve-fitting scheme used in our proposed method, it is capable of handling large benchmark circuits.

3. Methodology

3.1. Transistor Level Simulation

Use of the predictive model of degradation and recovery [14] to calculate the amount of threshold voltage shift of each transistor requires the knowledge of technology variables, temperature, and bias voltages (V_{dd} and V_{gs}). However, for a particular technology generation and operating temperature, the stress/recovery conditions are solely dependent on the V_{gs} bias of the PMOS transistors. The device is considered to be under *stress* if its V_{gs} is less than the threshold voltage V_{th} , otherwise it is assumed to be in *recovery*. If V_{gs} for a transistor can be inferred from the inputs to a gate, then the conditions for NBTI degradation can be easily deduced for any gate.

In this study, we look at two different models. The first is a simple model that is intuitive for logic level circuit simulations. This allows the PMOS gate to be in one of the two different states, namely *stress* or *recovery*. A PMOS gate is said to be under *stress* when its gate input is 0 and in *recovery* when its gate input is V_{DD} . This model holds

true for PMOS gates analyzed in isolation or in case of inverters and NAND gates which contain PMOS transistors in parallel in the pull-up stack. In these gates, the sources of all the PMOS transistors are tied to the supply voltage V_{DD} and hence V_{gs} is always either $-V_{DD}$ or 0. But for NOR gates with series stacked PMOS devices, the bias conditions depend on the transistor's input and also the states of other transistors in the stack. Extending the *2-state model* to NOR gates would lead to overly pessimistic calculations for threshold voltage degradation as some devices do not experience the maximum possible V_{gs} voltages.

In the extended *3-state model*, we aim to overcome the drawbacks of the simplistic model. SPICE level simulations reveal the status of all PMOS transistors in the pull-up network and their individual exact bias conditions. Details of these evaluations for all possible gate input combinations for various gate types are discussed in conjunction with Tables 1, 2 and 3 in the Results section. However, we explain below the basics for a three input NOR gate shown in Figure 1. Consider the PMOS transistor M_B in a stack. This can be in three different states as follows:

- **Stress:** In Figure 1a) the transistor M_A is ON and as a result M_B experiences a V_{gs} close to $-V_{DD}$ and hence is under complete *stress*.
- **Recovery:** There are two conditions under which a device can be in recovery.
 - Device input is V_{DD} : In Figure 1b) input B is high, hence V_{gs} for M_B is greater than the threshold voltage, therefore it is said to be in *recovery*. Here the stress condition is independent of the states of other transistors in the PMOS stack.
 - Device input is 0: In Figure 1d) transistor M_A is OFF, while M_B and M_C are ON. The sources of both the ON transistors have a direct path to ground and as a result the source node voltages are pulled below V_{th} and as a result the V_{gs} for both these devices (M_B and M_C) are greater than the threshold voltage. Consequently both M_B and M_C are in recovery.
- **Moderate Stress:** In Figure 1c) M_B is ON with M_A and M_C OFF. The source of M_B does not experience the complete supply voltage V_{DD} . Also the source has no discharge path to the ground and hence has a significant voltage but it is still less than V_{DD} . Here M_B is assumed to be under *moderate stress*.

The important deduction here is that the state of a device can be determined by absence or presence of direct paths to the supply lines. These in turn can be determined by the gate inputs, providing us a method to evaluate stress conditions accurately from current gate inputs. To check for con-

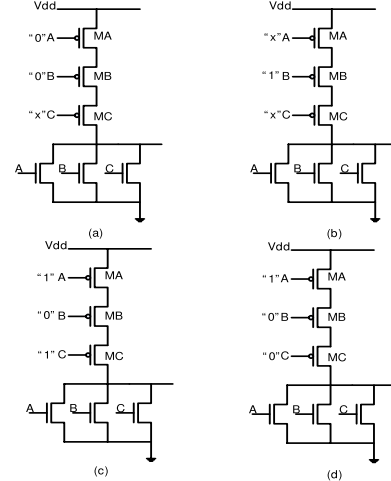


Figure 1. States for a PMOS transistor

sistency and validity of the extended model, SPICE simulations were performed for the 90nm, 65nm, 45nm and 22nm nodes. These nodes were selected because NBTI degradation is dominant only for sub-130nm nodes. The SPICE models for these nodes were based on the Predictive Technology used in [14]. The Vdd values used were 1.2V for 90nm and 65nm nodes, and 1V for the 45nm and 22nm nodes. Simulations were performed for 2, 3 and 4 input NOR gates by feeding the gate inputs through inverters and also loading the gate output with an inverter representing a fanout-factor of 3. In our experiments, each NOR gate was applied all possible combinations and only one signal was changed (swing signal). It was observed that the stress, moderate stress and recovery conditions for the PMOS transistors are consistent across the technology generations.

3.2. Gate Level Simulation

We designed and implemented a simulator that uses the *3-state model* described in the transistor level simulation subsection. The simulator can calculate PMOS transistor NBTI degradation under stress, moderate stress, or recovery phase, in large digital circuits. Further, to determine the long term threshold voltage degradation we use regression method in which we express the degradation by the power law given below:

$$\Delta V_t(t) = \alpha t^n \quad (5)$$

One could argue to use regression for the complete circuit degradation but, as demonstrated in many of the previous works [3], [17], [14], the circuit degradation is difficult to quantify using closed form approximations. Note that in the above equation, α and n are functions of various operating parameters like temperature, supply voltage, probability of stress and device parameters like gate oxide thickness and threshold voltage. The power law gives us a way of estimating the V_t degradation over the lifetime if stable values for α and n can be found.

Figure 2 shows the simulation methodology. It consists of two phases

- *Cycle accurate degradation simulation:* This phase carries out a cycle accurate simulation of NBTI degradation of all PMOS devices over a small fraction of the lifetime of the circuit. It is used to determine the values of α and n for all the PMOS devices statistically, by curve fitting, using the *least square fitting* method. In practice the new values need to be calculated on per cycle basis. Once we have the stable values of α and n for all PMOS devices, this phase is terminated. Another salient feature of this method is that the simulation can be carried out for any workload condition.
- *Long Term V_{th} degradation estimation:* Values of α and n obtained in the previous phase are used to estimate the long term V_{th} degradation using Eqn (5). This helps avoid cycle-by-cycle simulation over the entire lifetime of the circuit and makes the use of the simulator for large circuits feasible. The degradation in device delay can be estimated by using Eqn(4).

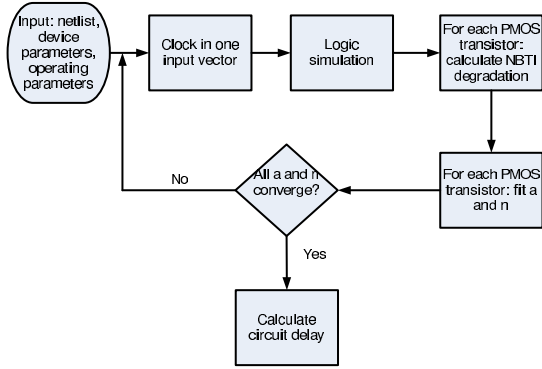


Figure 2. Simulation Methodology Flowchart

Finally, the path delay degradation can be calculated by analyzing the paths and these are taken as an indication of performance degradation of the circuit.

4. Results

The stress models and simulation methodology were evaluated for various ISCAS'85 and MCNC'91 circuits. These circuits were mapped to 2, 3, and 4 input NOR and NAND gates, and inverters. Unless stated otherwise, the simulations were carried out for operating temperature of 100°C and $f=1\text{GHz}$ and the device parameters with $V_{DD} = 1.2\text{V}$, $V_{th} = 200\text{mV}$ using the 65nm technology nodes.

4.1. Transistor Level Simulation Results

Tables 1, 2, and 3 show the results of SPICE simulations and bias voltages for the 2, 3, and 4 input NOR gates for the 65nm nodes. In these tables M1, M2, M3, etc denote the

PMOS transistors in the pullup stack. Further, the transistor M1 is assumed to be closest to the power supply. All voltage levels of less than 10mv in magnitude have been represented as zero. From the bias conditions it is apparent that the application of a 2-state model to identify stress/recovery conditions might lead to pessimistic evaluations. It is also seen that for the 3-state model, a device with gate input of 0 experiences significant reverse bias when its paths to V_{DD} and GND are cutoff, and almost negligible bias when cutoff is only from V_{DD} .

Table 1. V_{gs} Values for a 2-Input NOR Gate

INPUT LOGIC LEVEL		V_{gs} (V)	
M1	M2	M1	M2
0	0	-1.2	-1.2
0	1	-1.2	0.12
1	0	0	-0.13
1	1	0	0.36

Table 2. V_{gs} Values for a 3-Input NOR Gate

INPUT LOGIC LEVEL			V_{gs} (V)		
M1	M2	M3	M1	M2	M3
0	0	0	-1.2	-1.2	-1.2
0	0	1	-1.2	-1.2	0
0	1	0	-1.2	0	-0.13
0	1	1	-1.2	0	0.26
1	0	0	0	-0.15	-0.07
1	0	1	0	-0.76	0.44
1	1	0	0	0.25	-0.11
1	1	1	0	0.03	0.29

Table 3. V_{gs} Values for a 4-Input NOR Gate

INPUT LOGIC LEVEL				V_{gs} (V)			
M1	M2	M3	M4	M1	M2	M3	M4
0	0	0	0	-1.2	-1.2	-1.2	-1.2
0	0	0	1	-1.2	-1.2	-1.2	0
0	0	1	0	-1.2	-1.2	0	-0.13
0	0	1	1	-1.2	-1.2	0	0.20
0	1	0	0	-1.2	0	-0.15	-0.09
0	1	0	1	-1.2	0	-0.85	0.34
0	1	1	0	-1.2	0	-0.14	-0.11
0	1	1	1	-1.2	0	0.02	0.23
1	0	0	0	0	-0.17	-0.12	-0.09
1	0	0	1	0	-0.81	-0.81	0.39
1	0	1	0	0	-0.86	0.33	-0.10
1	0	1	1	0	-1.06	0.13	0.23
1	1	0	0	0	0.20	-0.12	-0.03
1	1	0	1	0	0.02	-0.80	0.39
1	1	1	0	0	0.01	0.04	-0.01
1	1	1	1	0	0.01	0.04	0.26

The difference in V_{th} degradation estimations between the 2-state and 3-state model can be seen from Table 4 which compares degradations for 3 and 4 input NOR gates. While computing the values give in this table, we assumed an average value of $V_{gs} = 700\text{mv}$ for the moderate stress conditions. It is apparent from this table that the 2-state model overestimated the degradation in all 3 cases. The

application of this model to large circuits and the related results, including comparison of two and three states model, are presented in a later subsection.

Table 4. ΔV_{th} for 2- and 3-State Models

Circuit	ΔV_{th} DEGRADATION (mV)					
	2-state model			3-state model		
	Max	Min	Avg.	Max	Min	Avg.
NOR3	11.55	11.35	11.44	11.22	7.59	9.60
NOR4	11.47	11.34	11.40	11.48	6.70	9.57

4.2. Validation of Simulation Methodology

To verify our proposed simulation methodology, we compare our model with the reference model from [14]. We conducted experiments for 45nm, 65nm and 90nm technology nodes. All parameters are obtained from the predictive model of [14]. The NBTI degradation of an inverter is simulated for 10 years of operation. Since the model in [14] can only handle periodical stress case, input vectors generated are patterns of equal 1's and 0's, signifying a duty cycle of 50%. However, We must add that the proposed simulation methodology can handle arbitrary patterns.

Table 5. Param. Dependence and Rel. Error

Parameters	Maximum Error ($\times 10^{-3}$)		
	90nm	65nm	45nm
<i>Baseline</i>			
$T=100^\circ C$, duty cycle=50%	7.89	8.23	6.32
<i>Vary Temperature</i>			
$T=50^\circ C$	7.52	3.43	2.38
$T=75^\circ C$	8.65	3.94	2.89
$T=125^\circ C$	5.12	4.69	3.75
<i>Vary duty cycle</i>			
Duty cycle=33%	8.37	7.45	1.41
Duty cycle=66%	2.57	2.15	1.41
Duty cycle=75%	9.26	8.07	6.02
<i>Vary T_{ox}</i>			
$T_{ox}=1.5nm$	9.04	8.13	6.29
$T_{ox}=2.5nm$	7.22	6.00	4.19

The results of the comparison for various parameters are shown in Table 5. We use the 3-state model for simulation purposes, but for an inverter there will not exist any divergence from the 2-state model due to the absence of any stacking effect. This table shows the relative error in V_{th} shift of PMOS transistors using proposed model and the reference model. The relative error is defined as follows:

$$RelError = \frac{|\Delta V_{th,reference} - \Delta V_{th,proposed}|}{\Delta V_{th,reference}} \quad (6)$$

It is seen that the relative error between the reference and proposed model is less than 1% in all cases. We conclude that the proposed method gives an accurate estimation of NBTI degradation.

4.3. V_{th} Degradation of Benchmark Circuits

We now present the results of V_{th} degradation for various ISCAS'85 and MCNC'91 circuits using both the 2-state and 3-state models of stress/recovery conditions with $\beta = 1.3$ [1]. Table 6 shows the comparative values. We observe that generally the 2-state model provides a more pessimistic estimation of the threshold shift. We also note that significant variations between the two models are absent. This is so because variations are to be expected only in circuits that have a considerable percentage of 3 or 4 input NOR gates, whereas the mapping was initially done to favor NAND usage. However, we note that for the two circuits, $i3$ and $i4$, the deviation is substantial and we found that it is due to the fact that these circuits are NOR gate intensive and hence more prone to stacking effect.

Table 6. ΔV_{th} for 2-State and 3-State Models

Circuit	ΔV_{th} DEGRADATION (mV)					
	2-state model			3-state model		
	Min	Max	Avg.	Min	Max	Avg.
<i>c1355</i>	2.33	21.98	11.54	2.26	21.87	10.09
<i>c1908</i>	1.86	23.88	11.22	3.47	22.43	10.80
<i>c432</i>	6.36	19.85	10.54	6.37	18.52	10.18
<i>c499</i>	2.32	21.79	11.53	2.29	21.92	11.00
<i>i1</i>	2.07	26.46	11.40	2.03	25.94	10.87
<i>i2</i>	4.96	29.07	11.99	4.92	28.59	11.22
<i>i3</i>	4.43	23.42	11.45	3.55	22.60	10.14
<i>i4</i>	4.89	27.86	11.51	4.84	22.20	10.82
<i>i5</i>	4.83	17.09	10.46	5.01	17.13	10.46
<i>i6</i>	5.73	11.59	10.16	5.75	11.54	10.14
<i>i7</i>	5.77	22.35	11.38	5.73	22.34	10.60
<i>i8</i>	2.69	78.57	12.52	2.86	74.90	10.94
<i>i9</i>	4.17	26.90	11.37	4.17	26.83	10.26

4.4. Circuit Delay Changes

The threshold voltage degradation affects the performance by increasing delay of the gates (in the critical path). To quantify this effect, we used Eqn(4) to determine the delay degradation of all gates in a circuit after computing the threshold voltage change using 3-state model.

The table 7 shows the percentage delay degradation in the long path of the circuits. We used three different values of β in Eqn(4). All circuits present a delay degradation close to 1-2%. It should be noted that a V_{th} degradation of 10% over a 10 year period manifests itself as only a 2% degradation in gate delay with $\beta=1.3$. For larger values of β the degradation is larger. Another and equally important observation we made is that for some circuits, like *c1355* and *c499*, the critical paths changed between the original circuit and the NBTI degraded circuit. This shows that overdesign for NBTI cannot be targeted at critical paths alone but must consider other long paths in the circuit.

5. Conclusion

In this paper a 3-state stress/recovery model for NBTI degradation is proposed and its necessity is substantiated

Table 7. Delay Degradation along Critical Path

Circuit	% Delay Degradation		
	$\beta = 1.3$	$\beta = 1.5$	$\beta = 2.0$
<i>c1355</i>	1.83	2.11	2.83
<i>c1908</i>	2.02	2.34	3.14
<i>c432</i>	1.60	1.85	2.48
<i>c499</i>	1.87	2.17	2.90
<i>i1</i>	1.70	1.96	2.63
<i>i2</i>	2.03	2.34	3.14
<i>i3</i>	1.76	2.04	2.73
<i>i4</i>	1.80	2.08	2.79
<i>i5</i>	1.66	1.92	2.56
<i>i6</i>	1.50	1.73	2.32
<i>i7</i>	1.84	2.12	2.85
<i>i8</i>	1.83	2.12	2.83
<i>i9</i>	1.86	2.16	2.89

by SPICE simulations. A simulation methodology, which is accurate, efficient and tractable, is developed that uses the 3-state stress/recovery model. The results of the two models are compared. There is only a 1% divergence between the proposed and the reference simulation methodologies. We also used the 3-state model to quantify the delay degradation of benchmark circuits. The results show the overall delay degradation to be small. Consequently, the effect of NBTI on timing degradation in large circuits is still diminutive compared to the time period a consumer prefers to use the hardware which sharply decreases as new technologies become available.

Our present methodology does not take into consideration the dependence of stress and recovery conditions on the past inputs. The future work will consider refining the stress/recovery model to include the effects of the current and the previous gate inputs.

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